

Fig. 1 Prior art

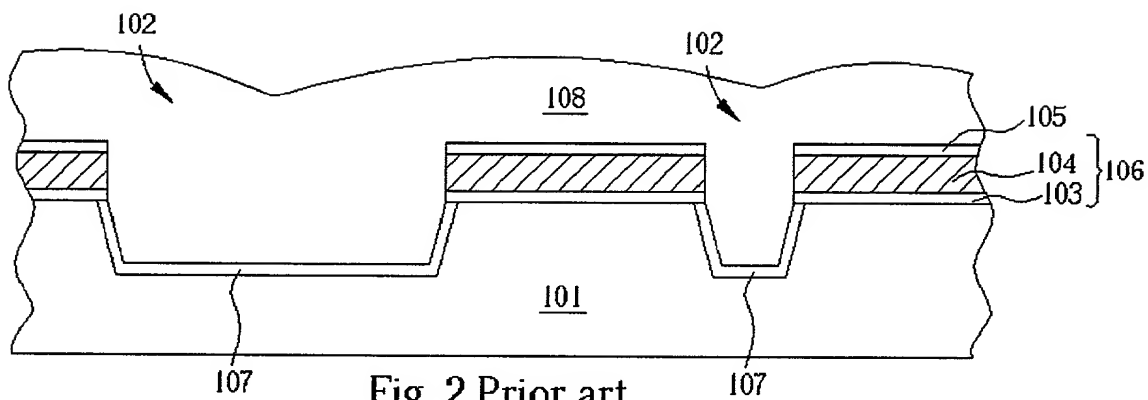


Fig. 2 Prior art

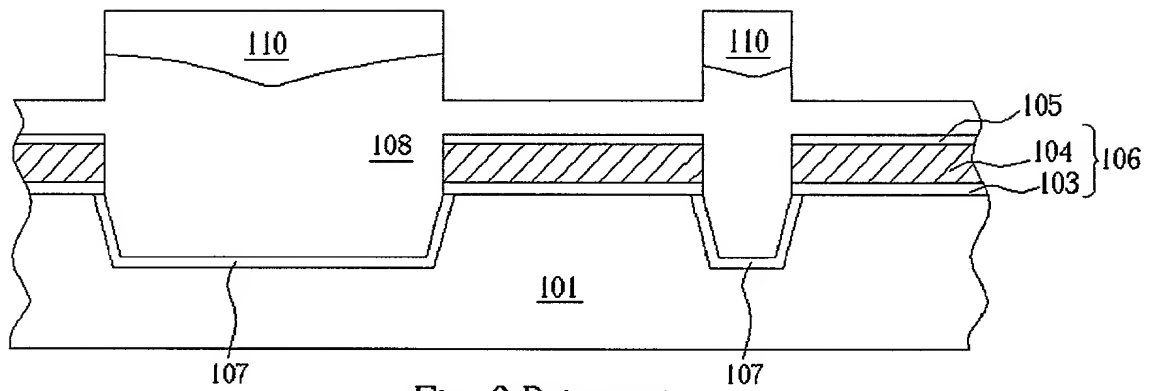


Fig. 3 Prior art

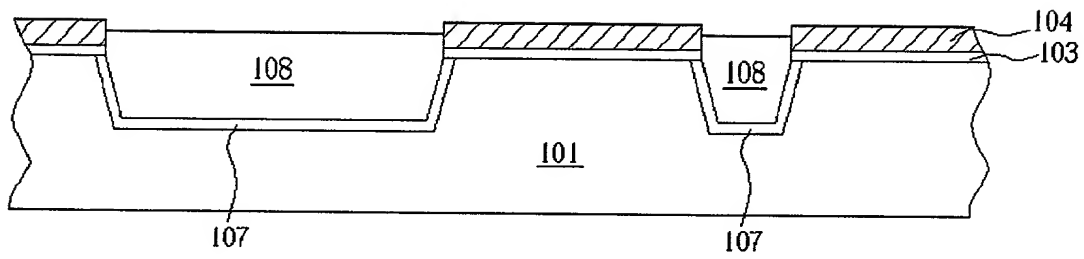
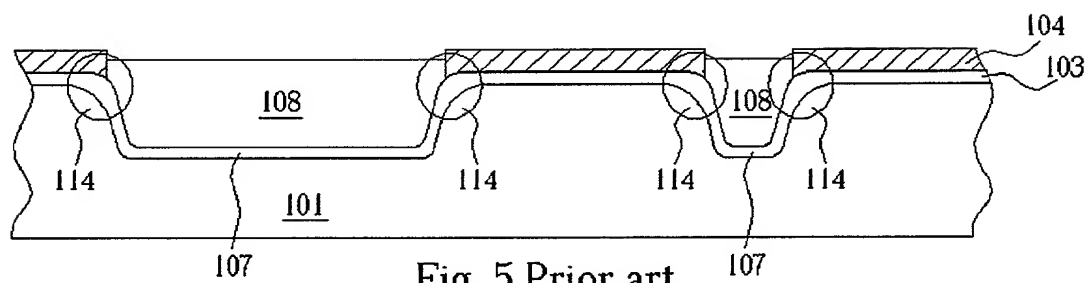


Fig. 4 Prior art



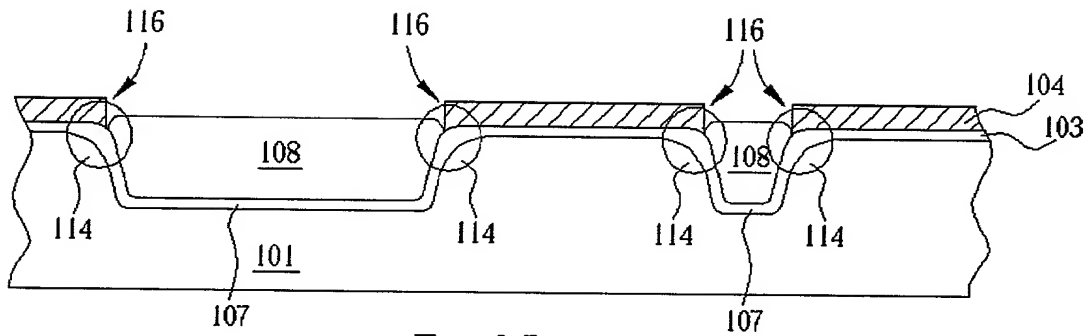
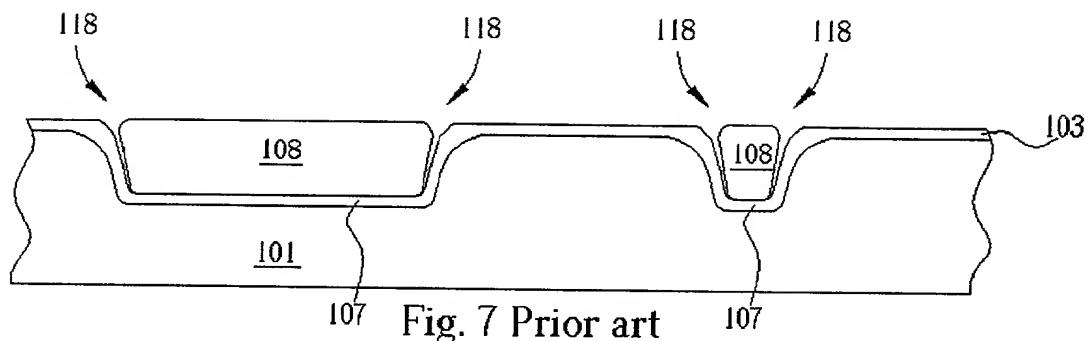


Fig. 6 Prior art



118 108 101 107 103

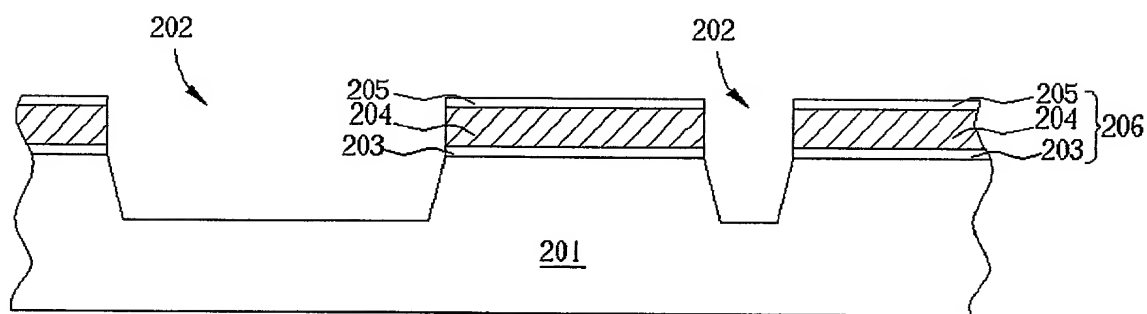


Fig. 8

FIG. 8 is a cross-sectional view of a semiconductor device. The device includes a substrate 201, a central region 202, and two side regions 202. The central region 202 is defined by a central portion of the substrate 201. The side regions 202 are defined by the portions of the substrate 201 on either side of the central region 202. The central region 202 is formed by a stack of three layers: a bottom layer 203, a middle layer 204, and a top layer 205. The top layer 205 is hatched. The side regions 202 are also formed by a stack of three layers: a bottom layer 203, a middle layer 204, and a top layer 205. The top layer 205 on the sides is also hatched. A bracket 206 groups the three layers (203, 204, 205) on the right side.



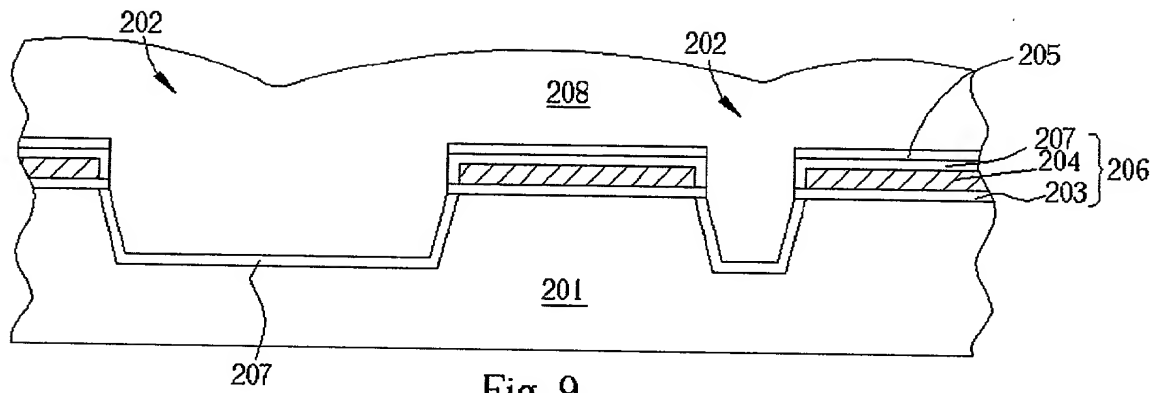


Fig. 9

FIG. 9 is a cross-sectional view of a semiconductor device structure. The structure includes a substrate 201, a central raised region 208, and side raised regions 205. The top surface of the central raised region is labeled 208, and the top surface of the side raised regions is labeled 202. The bottom of the side raised regions is labeled 207. The bottom of the central raised region is labeled 203. The top surface of the central raised region is labeled 204. The top surface of the side raised regions is labeled 206. The bottom of the side raised regions is labeled 207.

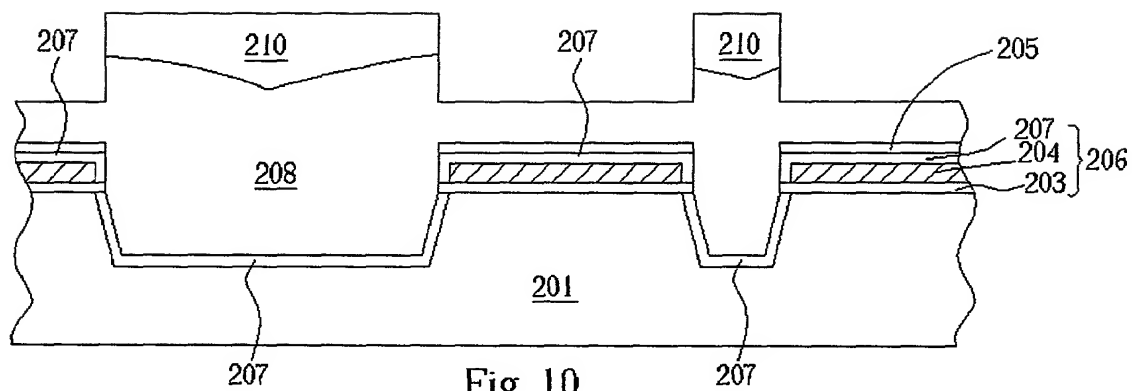


Fig. 10

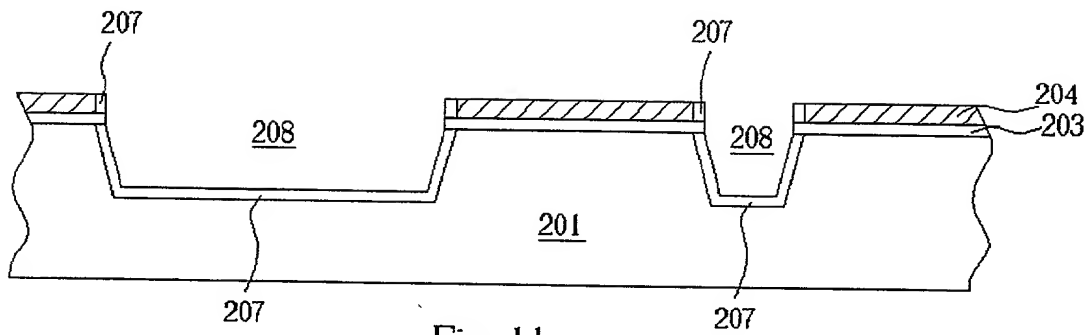


Fig. 11

FIG. 11 is a cross-sectional view of a device in accordance with the present disclosure. The device includes a substrate 201, a first layer 203, a second layer 204, and a third layer 208. The first layer 203 is disposed on the substrate 201, and the second layer 204 is disposed on the first layer 203. The third layer 208 is disposed on the first layer 203 and the second layer 204. The device further includes a first opening 207 and a second opening 207. The first opening 207 is formed in the first layer 203, the second layer 204, and the third layer 208. The second opening 207 is formed in the first layer 203, the second layer 204, and the third layer 208. The device is configured to perform a function.

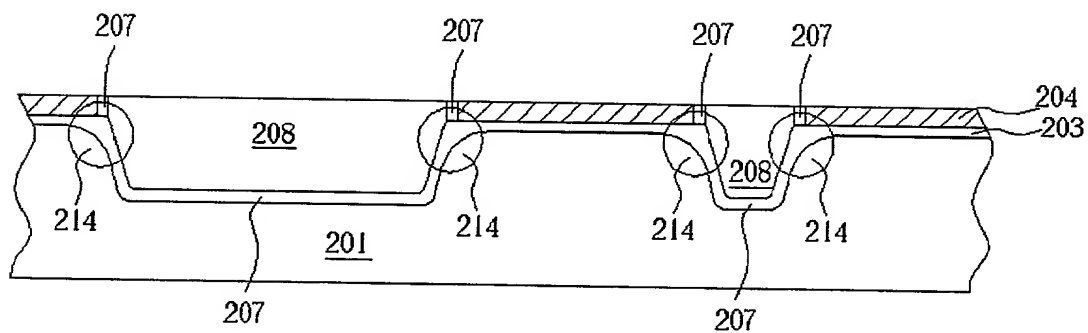


Fig. 12

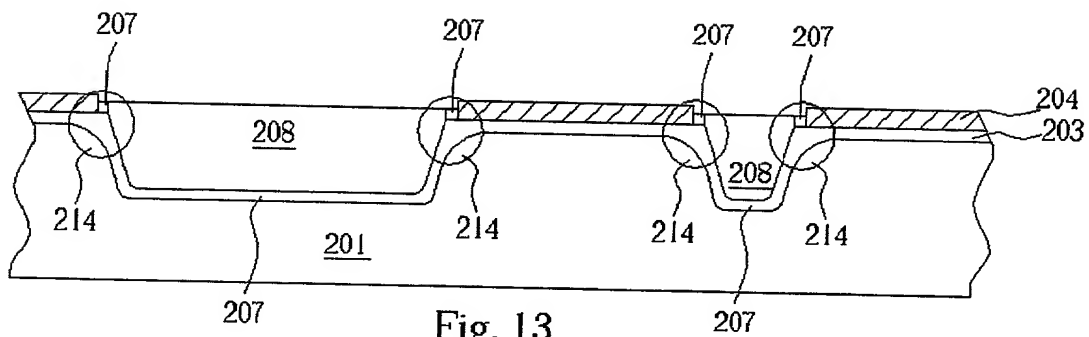


Fig. 13

FIG. 13 is a cross-sectional view of the device of FIG. 12, showing the device in a first state. The device includes a substrate (201) and a top layer (204). The substrate (201) has a series of rectangular cavities (208) formed therein. The top layer (204) is disposed on the substrate (201) and has a series of circular features (207) formed therein. The circular features (207) are positioned above the cavities (208). The device is shown in a first state, where the circular features (207) are in contact with the cavities (208).

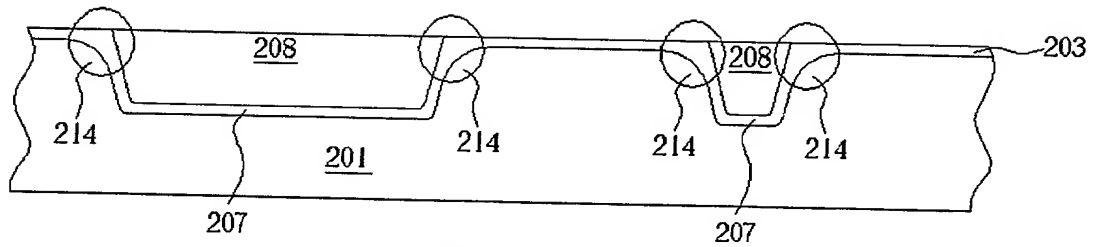


Fig. 14

FIG. 14 is a cross-sectional view of the device 100, showing the channel 201, the top layer 208, the bottom layer 207, and the side openings 214. The device 100 is shown with a wavy line indicating it is a partial view.